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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,073	10/17/2003	Yoshihiro Okada	81784.0287	8162

26021 7590 03/26/2008

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EXAMINER	
YEUNG LOPEZ, FEIFEI	
ART UNIT	PAPER NUMBER
2826	
MAIL DATE	DELIVERY MODE
03/26/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/688,073	OKADA ET AL.	
	Examiner	Art Unit	
	FEI FEI YEUNG LOPEZ	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The amendments submitted on 12/26/07 are acknowledged and entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Wada (US Patent 5,220,185).

3. Regarding claim 1, Wada teaches a solid image capturing element, comprising: a plurality of vertical shift registers (53 in fig. 5) arranged to each correspond to a column of a plurality of light receiving pixels (element 51 in fig. 5) in a matrix arrangement, a horizontal shift register (element 55 in fig. 5) provided on an output side of the plurality of vertical shift registers, and an output section (element 20 in fig. 1) provided on an output side of the horizontal shift register, wherein over one major surface of a semiconductor substrate of one conductive type, a first semiconductor region (n layer 23) of an opposite conductive type and a second semiconductor region (n+ layer 20) of the opposite conductive type and having a higher dopant concentration than that of the first semiconductor region are formed, the horizontal shift register is formed in the first semiconductor region (fig. 1 of a horizontal shift register, see column 5, lines 1-3); and the output section (output section layer 20) is formed in the second semiconductor region.

FIG.1

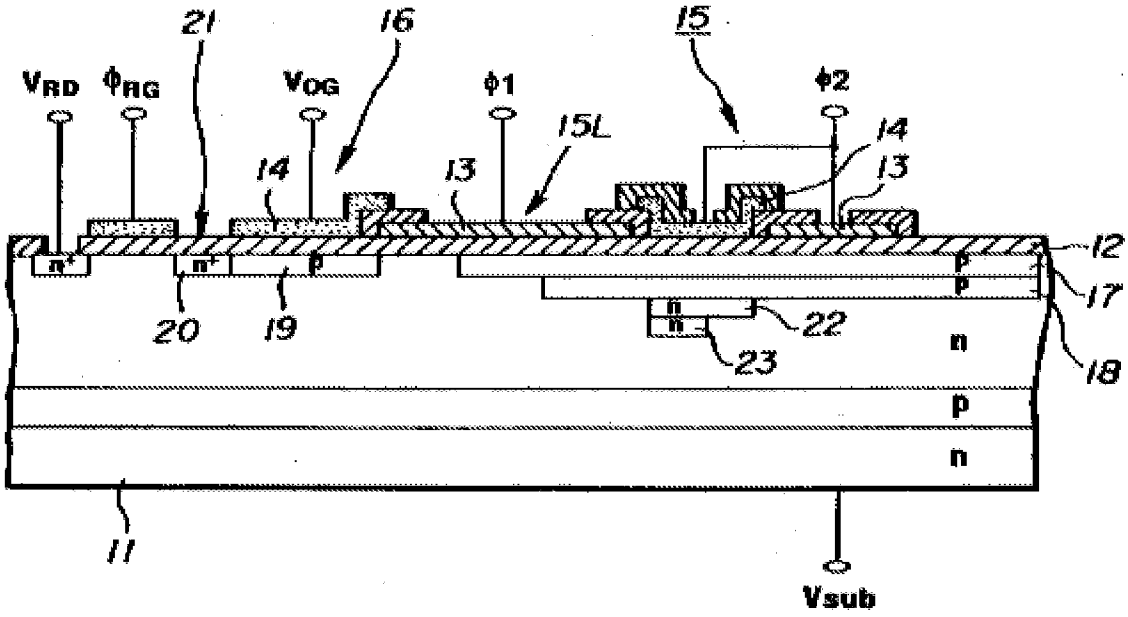
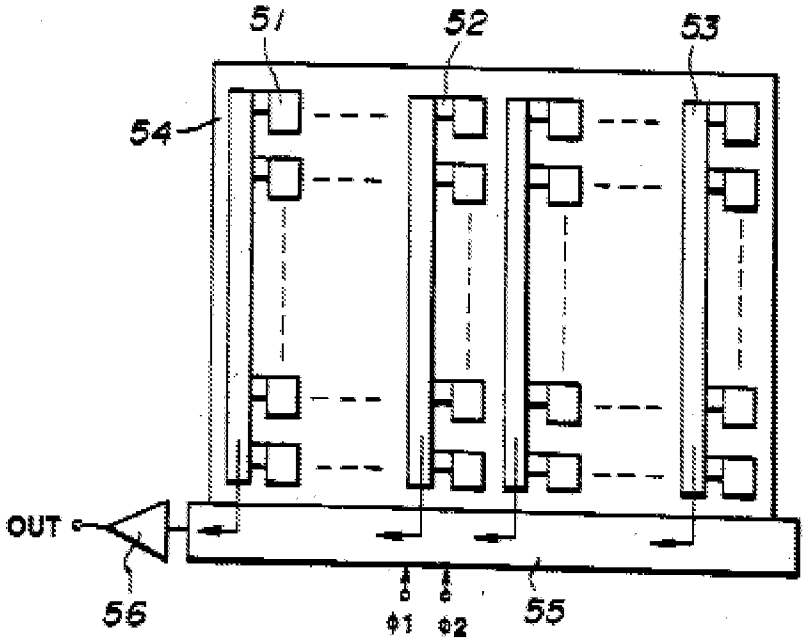

21
16
15
VRD
ΦRG
VOG
φ1
φ2
15L
14
13
14
13
12
17
18
20
19
22
23
n
p
n
11
Vsub

FIG. 5



4. Regarding claim 2, Wada teach the solid image capturing element according to claim 1, further comprising: an output gate (element 16 in fig. 1) formed on the semiconductor substrate at a boundary between the horizontal shift register and the output section.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada (US Patent 5,220,185) as applied to claim 1 above, and further in view of Yutani et al (US Patent 5,040,038), Oda (US Patent 4,805,026).

8. Regarding claim 3, Wada remains as applied in claim 1. However, Wada does not over the one major surface of the semiconductor substrate, a third semiconductor region of the opposite conductive type and having a lower dopant concentration than that of the first semiconductor region is formed, and the plurality of light receiving pixels and the plurality of vertical shift registers are formed in the third semiconductor region. In the same field of endeavor, Yutani teach over a major surface of a semiconductor substrate (p type substrate 1 in fig. 6A), a semiconductor region of the opposite conductive type of the substrate is formed (n^- vertical direction transfer channel 3) for the benefit of increase sensitivity (column 1, lines 10-12). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to make a n^- vertical direction transfer channel. And combining Wada with Yutani results in having a lower dopant concentration in the third semiconductor region (n^- vertical direction transfer channel 3) than that of the first semiconductor region for the benefit of increase

sensitivity. Moreover, and in the same field of endeavor, Oda teach a pixel made of n^- impurity concentration (pixel 30 in fig. 5(b), see column 2 ,lines 11-13, analogous to "a third region" claimed) for the benefit of providing an interline transfer type CCD area image sensor in a non-interlace scanning (column 2, lines 11-13). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the plurality of light receiving pixels and the plurality of vertical shift registers in the third semiconductor region, as taught by Yutani and Oda, for the benefit of providing an interline transfer type CCD area image sensor in a non-interlace scanning.

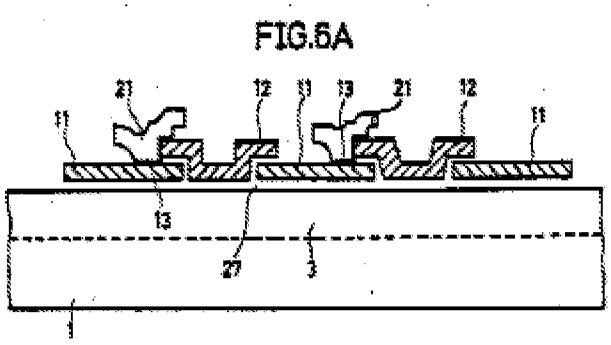


fig. 6A of Yutani

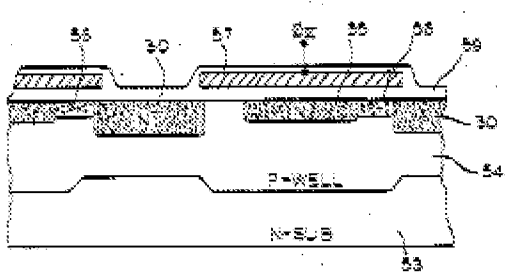


FIG.5(b)

fig. 5(b) of Oda

9. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada (US Patent 5,220,185) in view of Harada (US Patent 5,898,195).

10. Regarding claim 4, Wada teaches a method for manufacturing a solid image capturing element having a plurality of vertical shift registers arranged to each correspond to a column of a plurality of light receiving pixels in a matrix arrangement, a horizontal shift register provided on an output side of the plurality of vertical shift registers, and an output section provided on an output side of the horizontal shift register, comprising: a first step of forming over one major surface of a conductive semiconductor substrate (11 in fig. 3C) a first reverse conductive semiconductor region (17 in fig. 3A) having a first dopant concentration; a second step of forming over the one major surface of the conductive semiconductor substrate a second reverse conductive semiconductor region (19 in fig. 3B) having a second dopant concentration; and a third step of forming the horizontal shift register (on the right side of fig. 3C) on the first reverse conductive semiconductor region and the output section (on the left side of fig. 3C) on the second reverse conductive semiconductor region. However, Wada does not teach that the second dopant concentration is higher than the first dopant concentration. In the same field of endeavor, Harada teaches using a higher dopant concentration at a charge storage (element 7 in fig. 1, which is analogous to 19 in Wada's invention and the second dopant concentration as claimed) for the benefit of reducing dark current (column 1, lines 44-48). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the second dopant concentration higher than the first dopant concentration for the benefit of reducing dark current.

FIG. 3A

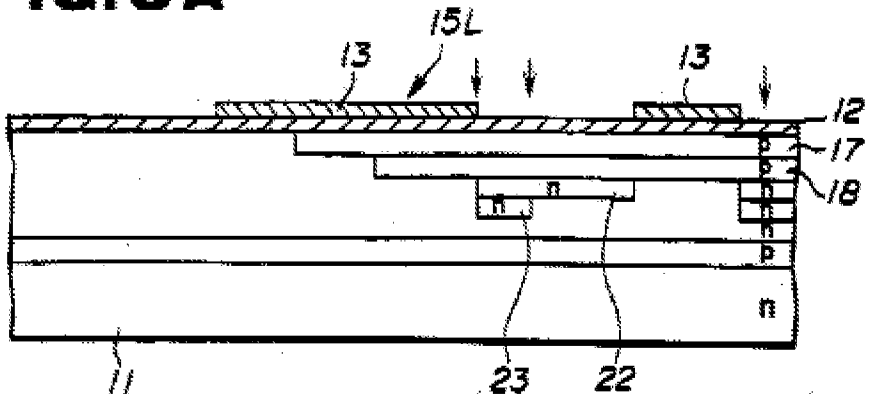


fig. 3A of Wada

FIG. 3B

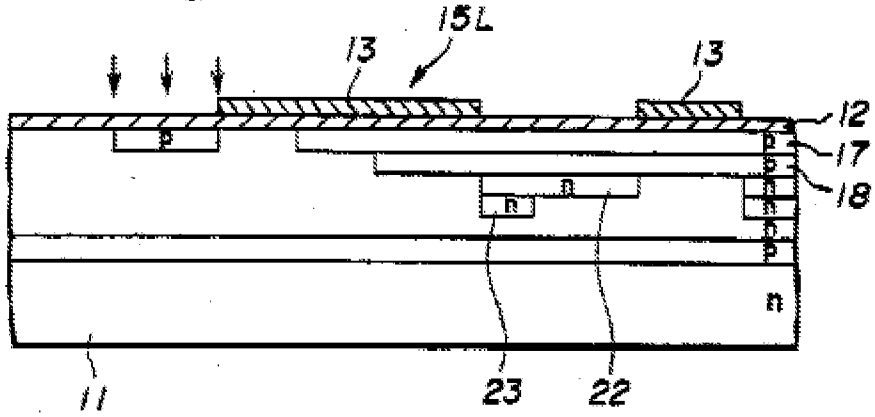


fig. 3B of Wada

FIG. 3C

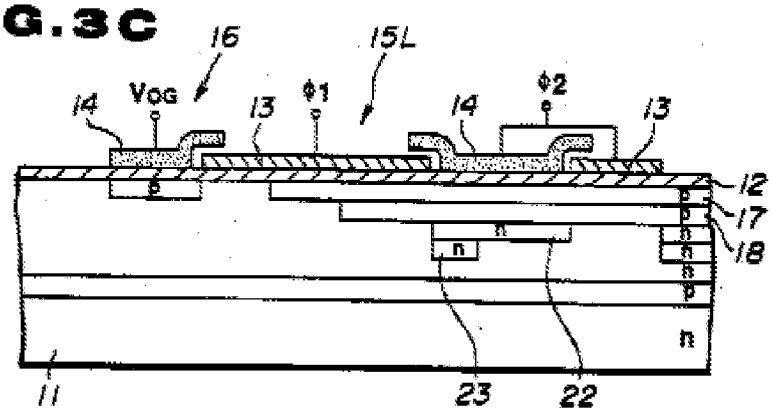


fig. 3C of Wada

FIG. 1

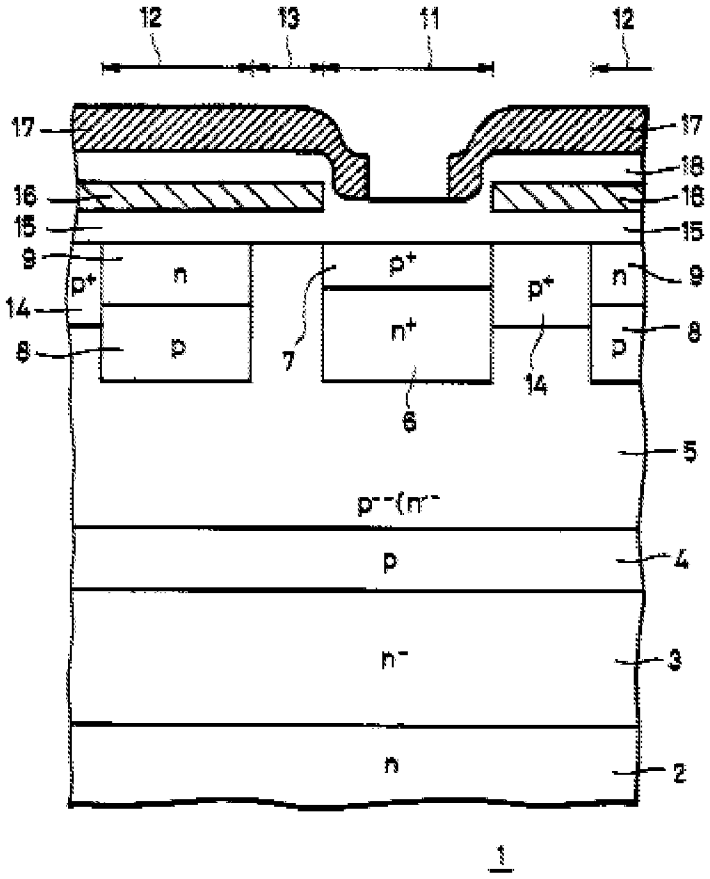


fig. 1 of Harada

11. Regarding claim 6, Wada teach that the method for manufacturing a solid image capturing element according to claim 4, wherein a dopant (n-type region on top of the p-type region, which contacts substrate 11, in figs. 3A-3C) is doped in a stepwise manner to the first reverse conductive semiconductor region and the second reverse conductive semiconductor region, and doping of the dopant is performed commonly at least once to the first reverse conductive semiconductor region, the second reverse conductive semiconductor region, and the third reverse conductive semiconductor region (note in

figs. 3A-3C and fig. 5 Wada teaches that the output section, the horizontal and the vertical shift registers, and the pixels are formed on the same substrate, therefore the n-type region is doped in all three regions at once.)

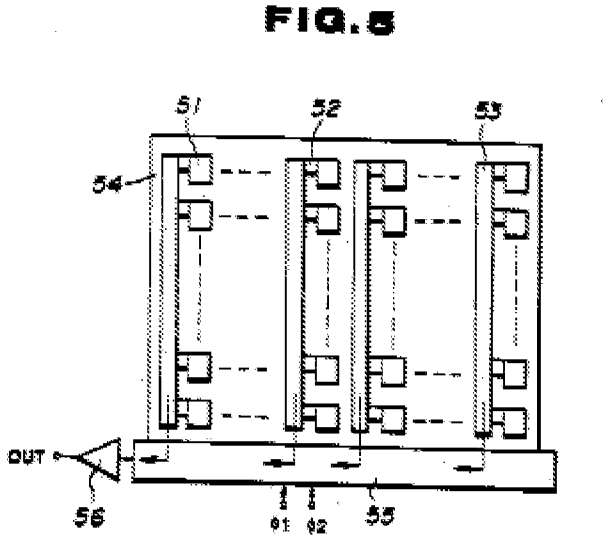


fig. 5 of Wada

12. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada (US Patent 5,220,185) in view of Harada (US Patent 5,898,195) as applied to claim 4 above, and further in view of Yamada (PG Pub 2002/0039144 A1), still further in view of Tohyama (US Patent 6,018,169).

13. Regarding claim 5, the previous combination remains as applied in claim 4. Furthermore, Harada teaches forming a light receiving pixel and a vertical shift register in a semiconductor region at one step (figs. 4A-4F). However, Harada does not teach a third dopant concentration lower than the first dopant concentration. In the same field of endeavor, Yamada teaches a dopant concentration in a vertical shift register region and

a pixel region are lower than that of a horizontal shift register region (see paragraphs [0010], [0022], [0023], and [0082]) for the benefit of making a smaller device (abstract). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to make a third dopant concentration lower than the first dopant concentration for the benefit of making a smaller device. Finally, also in the same field of endeavor, Tohyama teaches that a horizontal shift register should be made before a vertical shift register (column 16, lines 54-58) for the benefit of ease of production (abstract). Note that Harada teaches that a vertical shift register and a pixel can be made together (figs. 4A-4F).

FIG. 4A

FIG. 4B

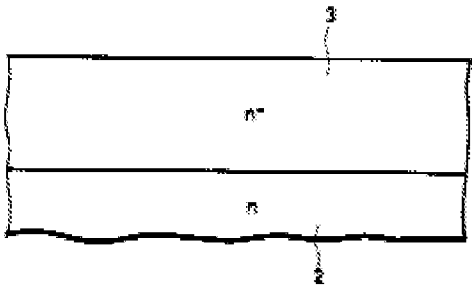


FIG. 4C

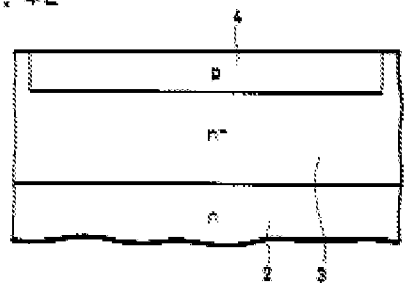


FIG. 4D

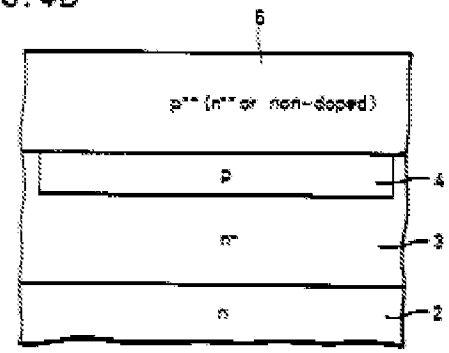


FIG. 4E

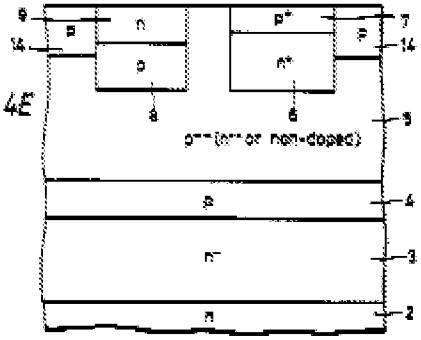
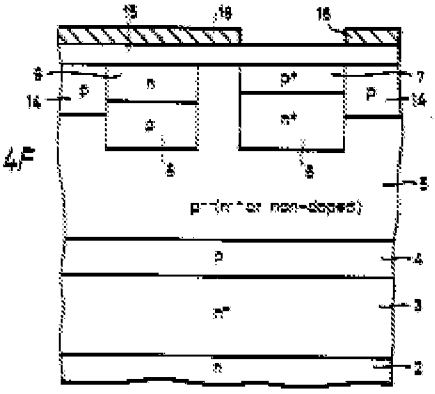


FIG. 4F



figs. 4A-4F of Harada

Response to Arguments

14. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is (571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Feifei Yeung-Lopez/

Examiner, Art Unit 2826

/Leonardo Andújar/

Primary Examiner, Art Unit 2826